What is claimed is:

1. A receiver adapted to detect an approximate value of the power of a reception signal, comprising:

first operation means for adding a value obtained by multiplying a smaller one of a component I and component Q of the reception signal by 1/8 and the value of a larger one of these components I and Q;

second operation means for adding a value obtained by multiplying the smaller one of the component I and component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one of these components I and Q by 7/8;

detection means for detecting the value of a larger one of the operation result of the first operation means and the operation result of the second operation means as an approximate value of the power of the reception signal.

2. A receiver adapted to detect an approximate value of the power of a reception signal, comprising:

a first comparator for comparing a component I and component Q of a reception signal with each other to determine which one of these components is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value;

a 3-bit shift register for multiplying the first output value from the first comparator by 1/8;

a subtractor for subtracting an output value from the 3-bit shift register from the first output value from the first comparator;

a 1-bit shift register for multiplying the second output value from the first comparator by 1/2;

a 2-bit shift register for multiplying an output value from the 1-bit shift register by 1/4;

a first adder for adding the first output value from the first comparator and the output value from the 2-bit shift register;

a second adder for adding an output value from the subtractor and an output value from the 1-bit shift register; and

a second comparator for comparing an output value from the first adder and an output value from the second adder with each other to determine which one of these output values is larger or smaller and output the value of a larger one thereof as an approximate value of the power of the reception signal.

3. A mobile-station device adapted to detect an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device including a receiver comprising:

first operation means for adding a value obtained by multiplying a smaller one of a component I and component Q of the reception signal by 1/8 and the value of a larger one thereof; second operation means for adding a value

obtained by multiplying a smaller one of the component I and component Q of the reception signal by 1/2 and a value obtained by multiplying a larger one thereof by 7/8; and detection means for detecting a larger one of the operation result of the first operation means and the operation result of the second operation means as an approximate value of the power of the reception signal.

4. A mobile-station device adapted to detect an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device including a receiver comprising: a first comparator for comparing a component I and component Q of a reception signal with each other to determine which one of these components is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value; a 3-bit shift register for multiplying the first output value from the first comparator by 1/8; a subtractor for subtracting an output value from the 3-bit shift register from the first output value from the first comparator; a 1-bit shift register for multiplying the second output value from the first comparator by 1/2; a 2-bit shift register for multiplying an output value from the 1-bit shift register by 1/4; a first adder for adding the first output value from the first comparator and the output value from the 2-bit shift register; a second adder for adding an output value from the subtractor and an output value from the 1-bit shift

register; and a second comparator for comparing an output value from the first adder and an output value from the second adder with each other to determine which one of these output values is larger or smaller and output the value of a larger one thereof as an approximate value of the power of the reception signal.

5. A detection method adapted to detect an approximate value of the power of a signal received from a receiver, comprising the steps of:

adding a value obtained by multiplying a smaller one of a component I and component Q of the reception signal by 1/8 and a larger one thereof to set the addition result to be a first operation result, adding a value obtained by multiplying the smaller one of the component I and component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one thereof by 7/8 to set the addition result to be a second operation result, and detecting a larger one of the first operation result and the second operation result as an approximate value of the power of the reception signal.

6. A detection method adapted to detect an approximate value of the power of a signal received from a receiver, comprising the steps of:

comparing a component I and component Q of the reception signal with each other to determine which one of these components is larger or smaller through the operation of a first comparator, to thereby output a larger

component as a first output value and output a smaller component as a second output value; multiplying the first output value from the first comparator by 1/8 through the operation of a 3-bit shift register; subtracting an output value from the 3-bit shift register from the first output value from the first comparator through the operation of a subtractor; multiplying the second output value from the first comparator by 1/2 through the operation of a 1-bit shift register; multiplying an output value from the 1-bit shift register by 1/4 through the operation of a 2-bit shift register; adding the first output value from the first comparator and the output value from the 2-bit shift register through the operation of a first adder; adding an output value from the subtractor and an output value from the 1-bit shift register through the operation of a second adder; and comparing an output value from the first adder and an output value from the second adder with each other through the operation of a second comparator, to thereby determine which one of these output values is larger or smaller and detect the value of a larger one thereof as an approximate value of the power of the reception signal.

7. A receiver adapted to detect an approximate value of the power of a reception signal, wherein:

operations are performed using a plurality of approximate equations, a plurality of candidates each becoming an approximate value of the power of the reception

signal are calculated, and an excellent one is detected from among a plurality of the candidates as an approximate value of the power of the reception signal.

8. A mobile-station device adapted to detect an approximate value of the power of a signal radio-received from a base-station device, comprising a receiver that performs operations using a plurality of approximate equations, calculates a plurality of candidates each becoming an approximate value of the power of the reception signal, and detects an excellent one from among a plurality of the candidates as an approximate value of the power of the reception signal.

9. A detection method adapted to detect an approximate value of the power of a signal received from a receiver, comprising the steps of:

performing operations using a plurality of approximate equations, calculating a plurality of candidates each becoming an approximate value of the power of the reception signal, and detecting an excellent one from among a plurality of the candidates as an approximate value of the power of the reception signal.